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REFAC electronics corporation

Manufacturers of OPTEL® Products

ENGINEERING BULLETIN

Bulletin No. OP-1

New Product _____

Technical Specification _____

Subject: Decoder Drivers For Liquid Crystal Displays

Page 1 of 14

Effective Date 4/1/79

Applies to: OPTEL Clock, Instrument, and Alphanumeric Liquid Crystal Displays

Rev. Date _____

Introduction

The Optel line of numeric and alphanumeric displays is versatile enough in terms of size and performance characteristics to be considered for a wide variety of clock, instrument and general purpose information displays. The advantages of these displays are most apparent in portable applications because of the extremely low power drain of the liquid crystal display (LCD) and in those applications where large size is required under a wide variety of ambient lighting conditions. This diversity of applications leads to a wide variety of interface conditions where the output of devices such as microprocessors, analog-to-digital (A/D) converters, metering devices, serial data streams, etc., must be converted to the special format necessary to drive the LCD. The object of this bulletin, therefore, is to provide sufficiently detailed information which will enable users of Optel LCD's to operate them at optimum levels of performance and reliability.

Drive Requirements of Field Effect Liquid Crystal Displays

A necessary requirement for long display life (>50,000 hours) is that the net DC voltage across any LCD segment is zero. This is most easily accomplished by applying a square wave drive voltage to the backplane of the display and supplying a square wave of the same frequency as the backplane to each segment but either in phase for an OFF segment or out-of-phase for an ON segment. The appropriate waveforms for the ON and OFF conditions are shown in Figure 1 (a).

In a practical situation, the digital signals that are to be displayed are stored as logic levels, i.e., "0" (OFF) = volts and "1" (ON) = + V_{DD} volts. A convenient means of converting these levels to the appropriate phase square wave makes use of an EXCLUSIVE OR gate such as the CD 4030 as shown in Figure 1 (b). One of the inputs to the gate is the backplane square wave and the other is the logic level so that a high level creates out-of-phase square wave necessary to turn the segment ON and vice-versa. As described in Bulletins OP-100, OP-101 and OP-102, the required

drive voltages are 2.5 - 15 volts rms corresponding to peak square wave voltages of 2.5 - 15 volts. This is completely compatible with micro-power CMOS circuitry which operates from 3-18 volts. Recommended drive frequencies range from 30-100 Hz.

Interface Circuit Recommendations

Most realistic systems, e.g., clocks, DVM's, meters and general purpose information displays incorporate a number of characters and at 7-14 segments per character, the number of drivers can become quite large. Thus, the use of discrete EXCLUSIVE OR drivers is prohibitive because of cost and the complexity of interconnection. Fortunately, there are several CMOS MSI devices available which simplify the system designers job considerably by providing LCD compatible drive signals as well as circuitry that interfaces with standard digital codes. The following examples represent typical display interfaces and give specific CMOS circuit realizations.

a. Numeric Data - Binary Coded Decimal (BCD)

The most widely used digital code for numeric data is Binary Coded Decimal or BCD, where the 4 bit binary numbers are mapped into the decimal digits 0 through 9 (the binary numbers corresponding to 10 through 15 are invalid). There are several CMOS MSI devices which provide the necessary storage, decode, and drive functions for a seven segment LCD. The RCA CD 4056 or the MITEL MD 4056 are good examples of such devices and are illustrated in block diagram form in Figure 2. The 4056 is a single digit BCD-7 segment decoder/driver and provides outputs which directly drive the seven segments of a LCD. The driver outputs are controlled by the square wave display frequency input which causes the segments to be in or out of phase when unselected or selected by the BCD input. The truth table of Figure 3 shows the relationship between the BCD inputs and the 7 segment outputs and also illustrates the displayed character. There is in addition, a strobed latch feature which gates the signals on the input lines into memory when the STROBE line goes high and permanently stores this data when STROBE again goes low.

More than one digit can be driven with N 4056 devices from a common BCD data line by gating the individual STROBE lines, and using common DF IN lines (Figure 4). The oscillator circuit will produce a square wave at about 50 Hz.

As mentioned previously, care must be taken in the oscillator circuit in order to insure that the pulse train has exactly 50% duty cycle. A relatively simple oscillator can be implemented with 2 inverters, a resistor and a capacitor as in Figure 5 (a). The frequency $f \cong \frac{0.7}{RC}$ but the duty cycle can vary considerably depending on supply voltage and CMOS device parameters. Combining this basic oscillator with an edge triggered flip flop as in Figure 5 (b) produces the desired 50% cycle. In the specific implementation shown, the output of the inverter is a pulse train at 100 Hz and the display frequency output of the CD 4013 is half

this frequency or 50 Hz.

A preferred and more economical way of implementing the drive circuitry for 4 or greater digits uses the Silicomix DF 411 decoder/driver. This CMOS device contains all the necessary circuitry for storing, decoding and driving 4 LCD digits. The backplane oscillator is also incorporated on a chip so that all that is required is a single external capacitor connected from the OSC pin to ground (capacitor values of 390 pf to 1,000 pf are sufficient to generate the 30-100 Hz backplane frequency). Multiples of 4 digits can be driven by ganging more than one DF 411, decoding the digit strobe lines and driving the OSC pins in parallel with an external oscillator (Figure 6).

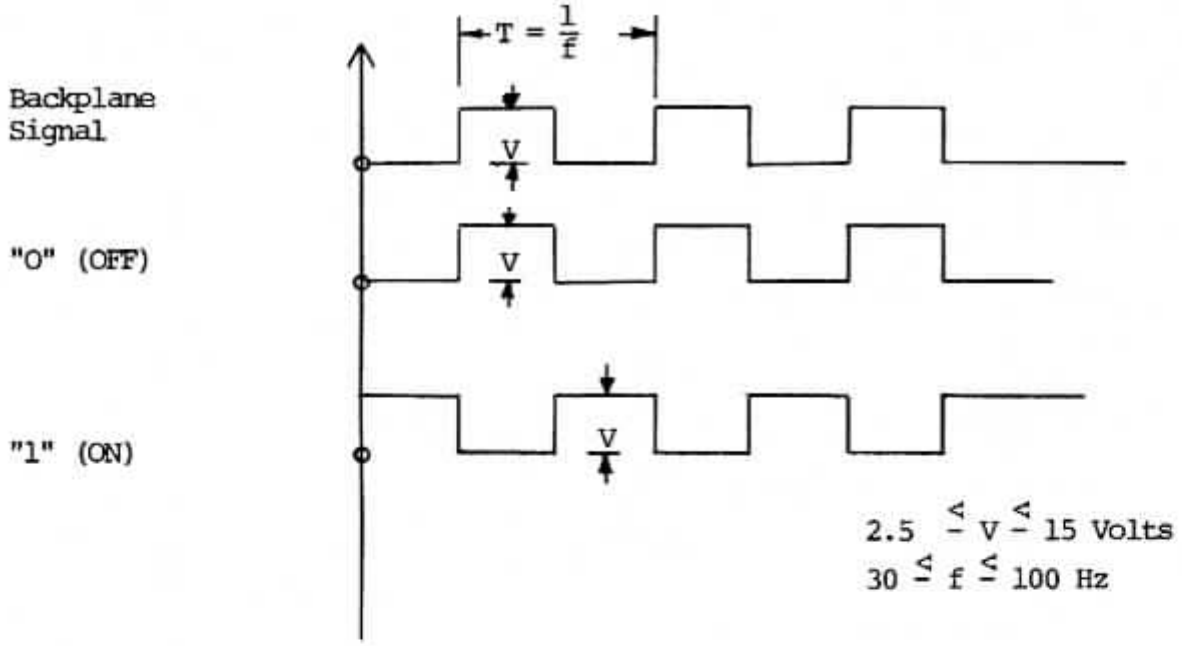
b. Numeric Data - Serial Input

In many applications involving remote communications, the display data is presented as a serial digital data stream and the use of the parallel BCD decoder/drivers discussed previously becomes inconvenient and therefore uneconomical. A serial IN parallel OUT shift register such as the MITEL 4331 and 4332 30 and 32 bit devices and the Hughes HLCD 0438 will perform this function. Each unit can accept and store serial data at rates ranging from DC to 3 MHz and drive up to four 7 segment numeric displays plus decimal points. The circuits accept serial data at DE and shift it into the register on the positive transition of the clock (CLK). The parallel outputs are available in either TRUE or complement form depending on the state of the T/C input, a feature which can be used to generate the AC drive for the display by supplying a low frequency (30-100 Hz) square wave to T/C and to the display backplane. The DO (Data OUT) line can be used to drive the DI input of another 4331 (4332) for displays larger than 4 digits. The block diagram of Figure 7 shows the use of the 4331 in driving an 8 digit display from an incoming serial data stream.

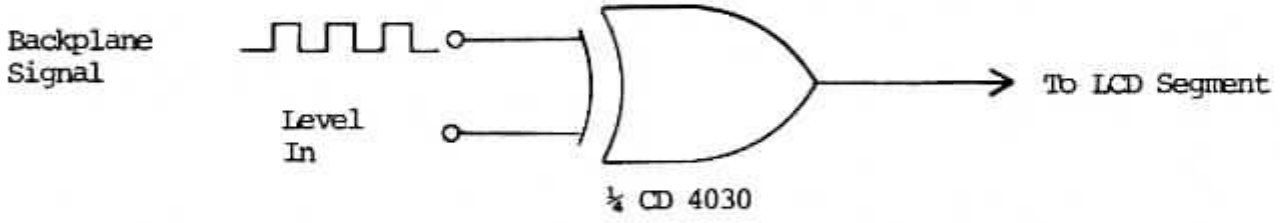
c. Alphanumeric Data - Hexadecimal and ASCII

In more sophisticated information processing systems, it is often necessary to decode and display alphanumeric information. Unlike numeric information where BCD IN and 7 segment OUT are the accepted standards, many different formats are employed for alphanumerics. The two most widely used, however, are hexadecimal and ASCII codes. Hexadecimal (or hex) is a binary code where the full range of 16 characters is generated from a 4 binary number. The characters corresponding to the binary numbers 1010 through 1111 (10-15) which are unused in BCD, are denoted by the letters A through F. The hex code is commonly used in most 8 bit micro processors where each byte (8 bit word) is represented by two hex digits ranging in value from 00 to FF. The hex output is of course a very limited form of alphanumeric display and can be displayed for example with the Optel LCD 65000 series in conjunction with the MITEL MD 4311 decoder driver as shown in Figure 8. The STROBE or LATCH ENABLE input can be used to gate information into the ON chip register. In an 8 bit microprocessor, two hex digits can be displayed by placing the 8 data lines onto the system lines and driving the STROBE signal in a memory mapped mode, i.e., treating the display and its associated 8 bit register as 1 byte of memory.

The full set of alphanumeric characters (upper case alphas plus numerics) can be displayed with the Optel 70000 series which are 16 segment LCD digits in the star burst format of Figure 9. Seven bit ASCII code is the accepted standard for alphanumeric information and generates the character set of Figure 10 when driven by the indicated 9 bit work. Decoding and driving such displays is obviously more complex than straight numeric displays as previously described. The drive circuitry can be implemented with the MITEL MD 4332 which is a 32 bit device and can therefore drive two 16 segment displays or two 14 segment displays plus decimal points. As with the MD 4331, the data input is bit serial. The decode function is usually accomplished within the associated microprocessor. In the case where the display is operating as a "stand alone" device, programmable ROM's can adequately perform this function. Further information can be obtained by consulting Optel Division of REFAC Electronics Corporation or your local representative.



(a) Drive Waveforms

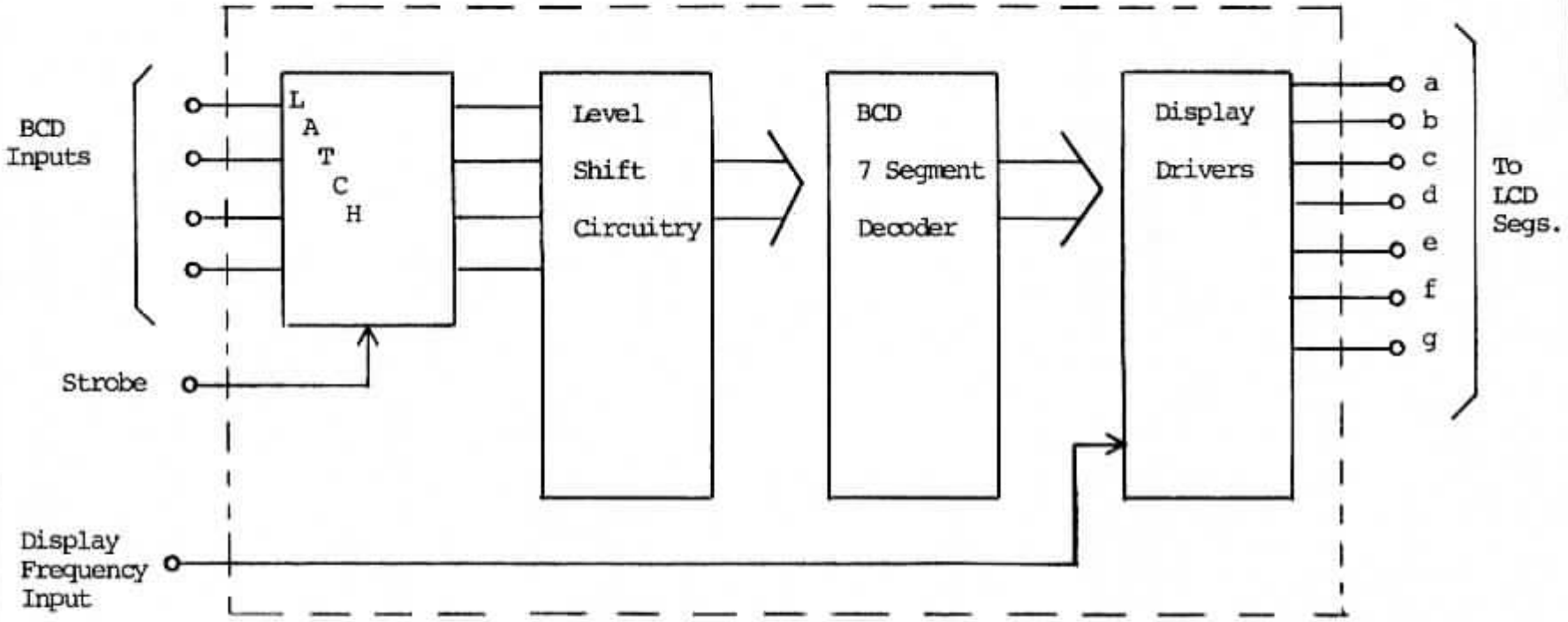


(b) Exclusive or Driver

FIGURE 1 - LCD DRIVE REQUIREMENTS

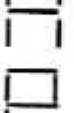
OPTEL DIVISION REFAC electronics corporation		DWG. NO. SHT 5 OF SHTS 14	REV

721215-2



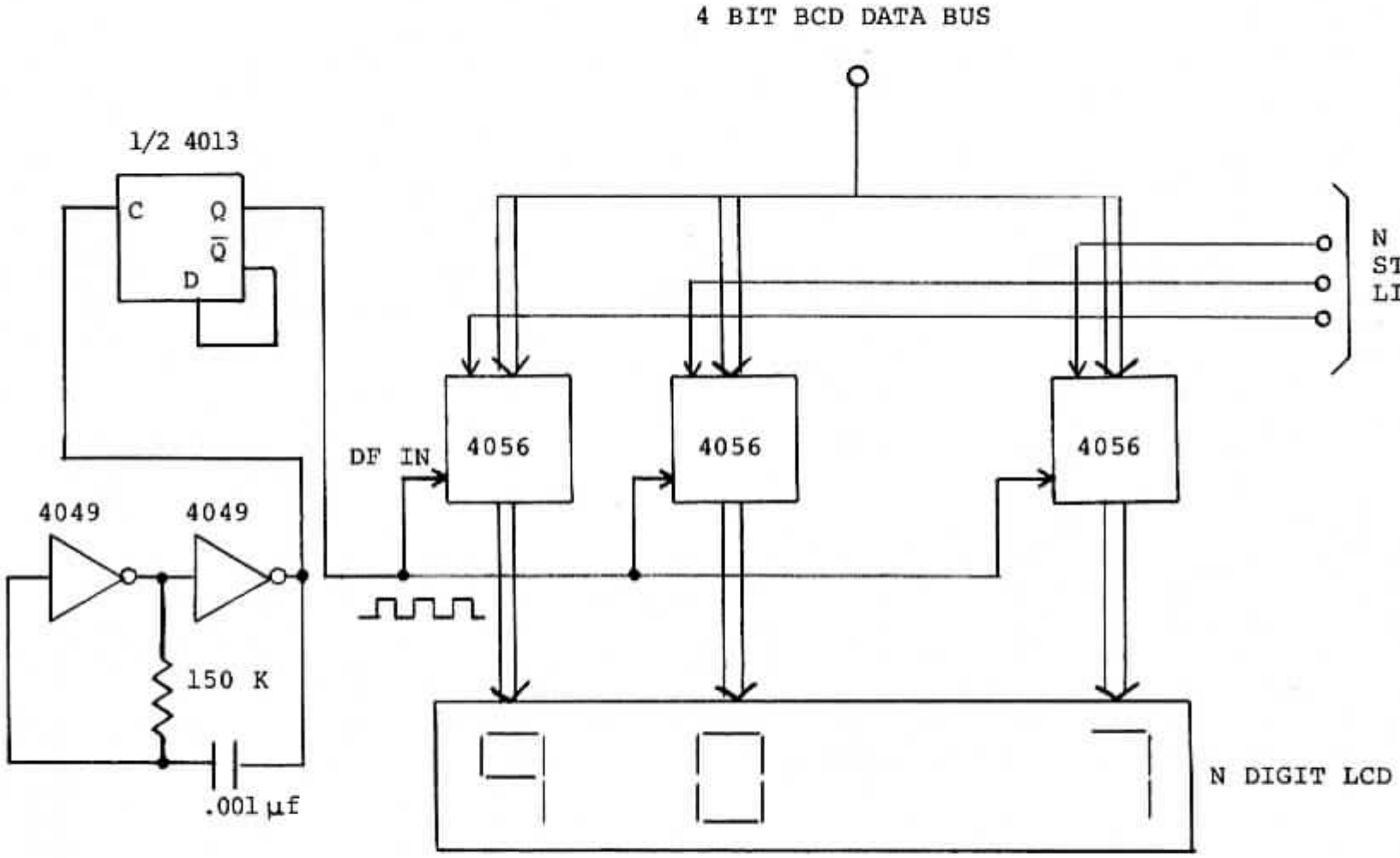
RCA CD 4056 or MITEL MD 4056

FIGURE 2 - BCD - 7 SEGMENT DECODER/DRIVER

INPUT	OUTPUT*	DISPLAYED CHARACTER
2^3 2^2 2^1 2^0	a b c d e f g	
0 0 0 0	1 1 1 1 1 1 0	
0 0 0 1	0 1 1 0 0 0 0	
0 0 1 0	1 1 0 1 1 0 1	
0 0 1 1	1 1 1 1 0 0 1	
0 1 0 0	0 1 1 0 0 1 1	
0 1 0 1	1 0 1 1 0 1 1	
0 1 1 0	1 0 1 1 1 1 1	
0 1 1 1	1 1 1 0 0 0 0	
1 0 0 0	1 1 1 1 1 1 1	
1 0 0 1	1 1 1 1 0 1 1	
1 0 1 0	0 0 0 1 1 1 0	
1 0 1 1	0 1 1 0 1 1 1	
1 1 0 0	1 1 0 0 1 1 1	
1 1 0 1	1 1 1 0 1 1 1	
1 1 1 0	0 0 0 0 0 0 1	
1 1 1 1	0 0 0 0 0 0 0	BLANK

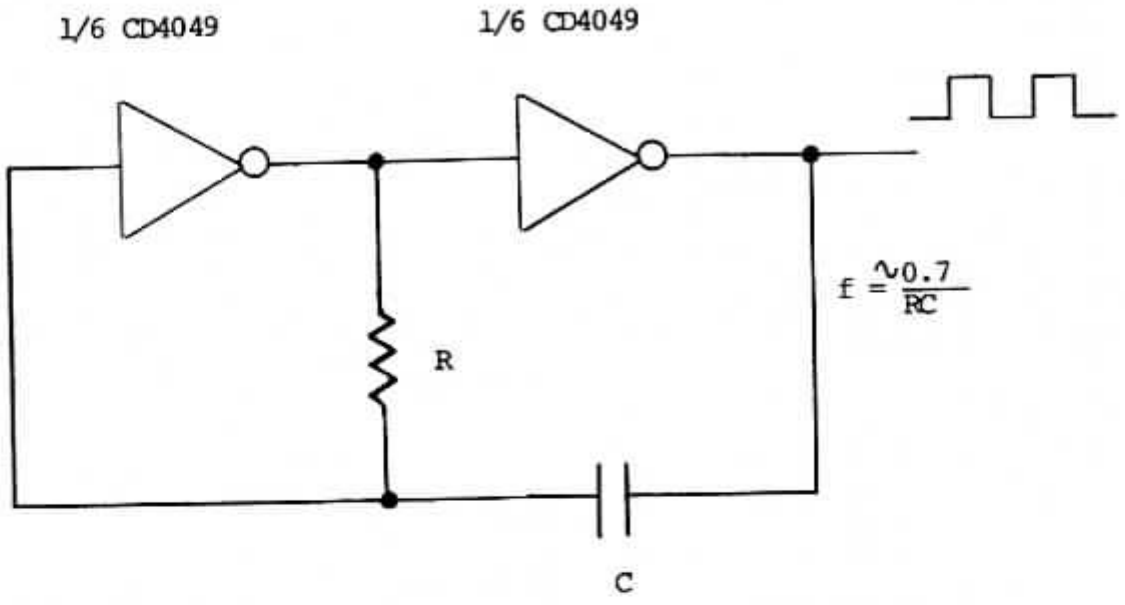
*ST - "1" = OUT OF PHASE SQUARE WAVE
"0" = IN PHASE SQUARE WAVE

FIGURE 3 - BCD - 7 SEGMENT TRUTH TABLE

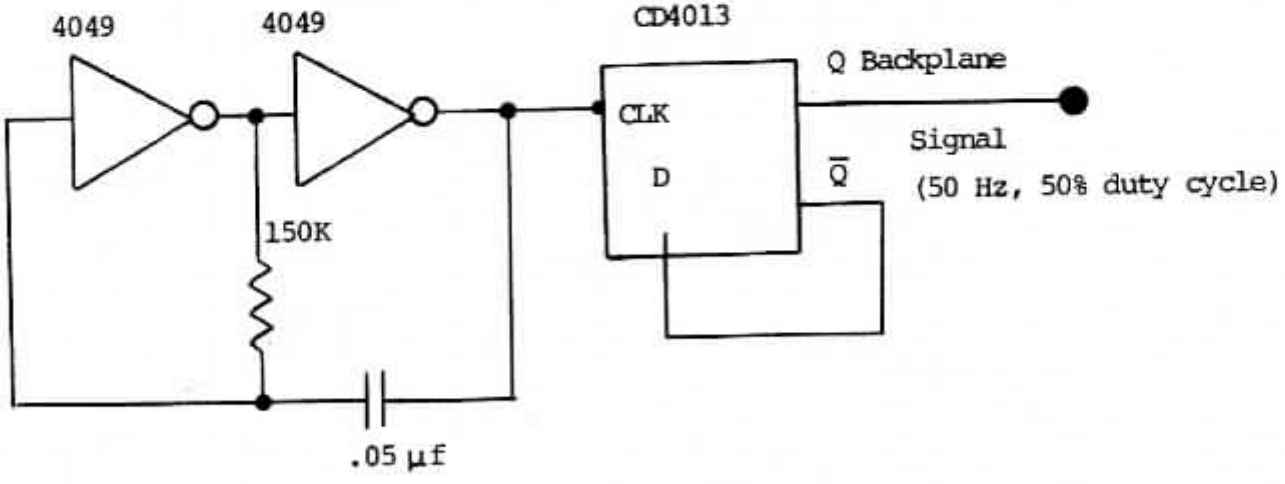


OPTEL NUMERIC DISPLAYS SERIES 65000

FIGURE 4 - N DIGIT DISPLAY DRIVE CIRCUITRY



(a)



(b)

FIGURE 5 - OSCILLATOR CIRCUITS

OPTEL DIVISION REFAC electronics corporation		DWG. NO. SHT 9 OF 14 SHTS	REV

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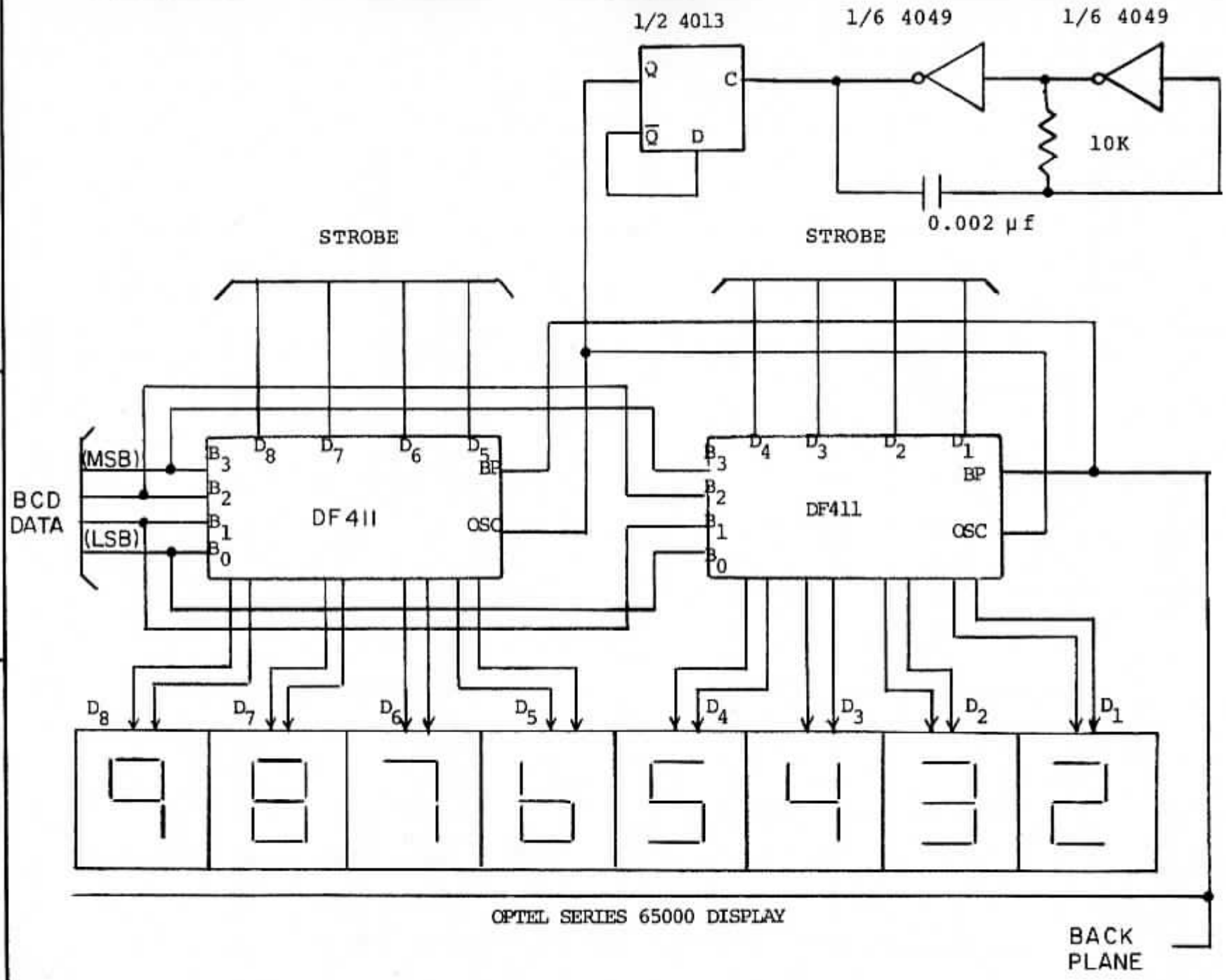

FIGURE 6 - 8 DIGIT LCD DRIVE CONFIGURATION

DWG. NO.
SHT 10 OF 18SHTS
REV

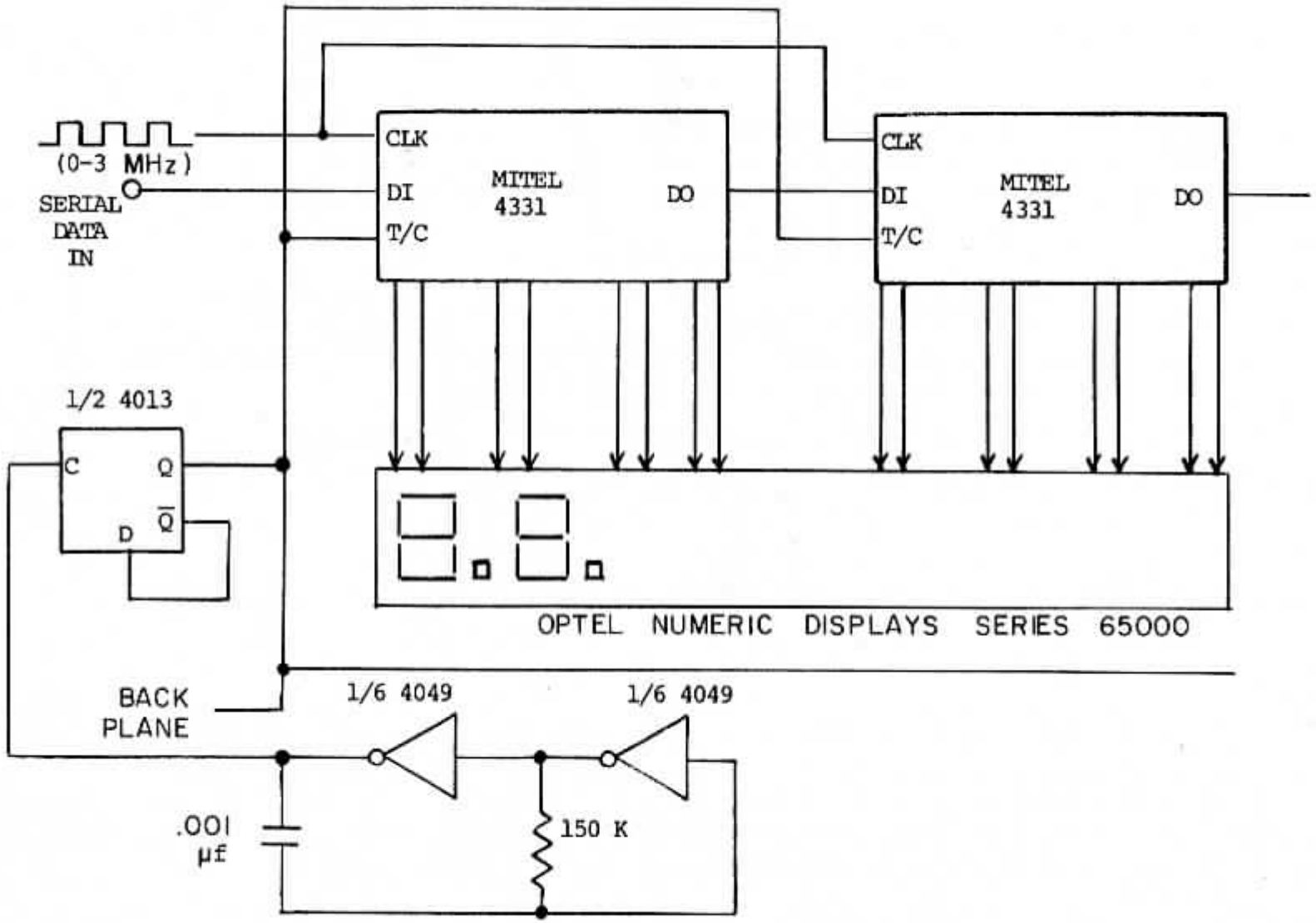

FIGURE 7 - SERIAL IN, PARALLEL OUT DRIVE

DISPLAY OUTPUT

BINARY INPUT	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111

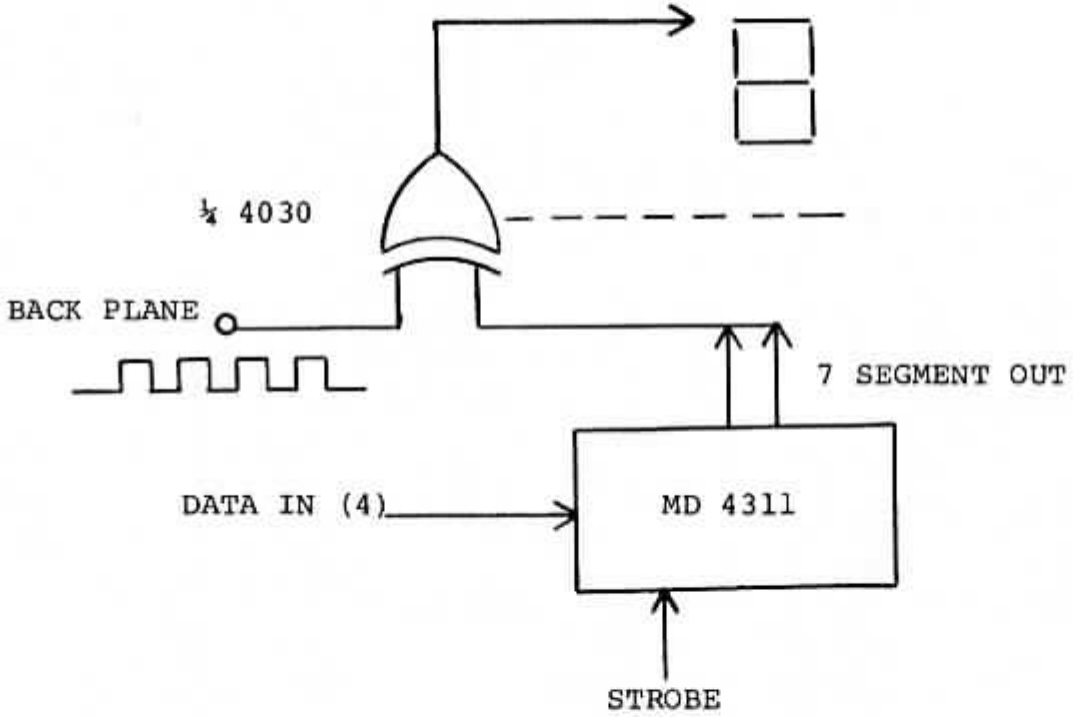

FIGURE 8 - HEXADECIMAL LCD DISPLAY

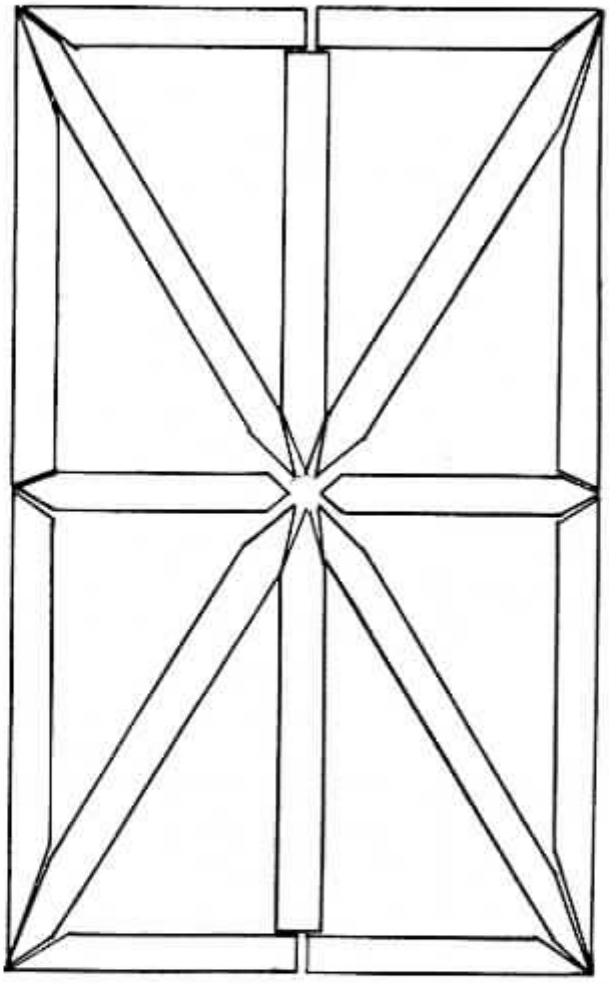

FIGURE 9 - 16 SEGMENT LCD CHARACTER

D0	0	1	0	1	0	1	0	1
D1	0	0	1	1	0	0	1	1
D2	0	0	0	0	1	1	1	1

D6 D5 D4 D3								
0 1 0 0								
0 1 0 1								
0 1 1 0								
0 1 1 1								
1 0 0 0								
1 0 0 1								
1 0 1 0								
1 0 1 1								

FIGURE 10 - ASCII CHARACTER SET AS CAN BE FORMED ON OPTEL SERIES 70000 DISPLAYS

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